REMARKS

Favorable reconsideration of this application in view of the foregoing amendments and remarks to follow is respectfully requested.

Applicants note that the Examiner stated, in the Office Action dated December 5, 2001, that Claims 29 and 30 are allowable subject matter over the prior art. Therefore, if the current §112 rejection is overcome applicants request that Claims 29 and 30 be allowed.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have amended Claim 24 to positively recite that the claimed poly-poly capacitor comprises planar upper and lower plate electrodes. Support for this amendment is found in FIG. 3 which depicts a planar poly-poly capacitor having a planar upper electrode (top plate) 42, a lower electrode (bottom plate) 26, spacers 28 56, STI region 12, and a substrate 10.

Claims 24-30 stand rejected under 35 U.S.C. §112, first paragraph, for allegedly containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make and/or use the invention. More specifically, it is the Examiner's position that the material "SiGe polysilicon" is impossible to make because polysilicon cannot be SiGe.

Applicants submit that depositing SiGe over an oxide-containing region forms SiGe polysilicon. The term "SiGe polysilicon" is used in the present invention to denote a polysilicon germanium layer. Referring to pages 15-16 and FIG. 1D, applicants disclose that a SiGe polysilicon layer 42 is formed atop a layer of polysilicon 34 over regions containing oxides, including the bottom insulating layer (oxide) 34 and shallow trench isolation region (oxide) 14. Additionally, applicants disclose, referring to page 12 of the present specification, that the insulating material of the bottom insulating layer 34 may be SiO_2, Si

oxynitride, and other like insulative materials. Referring to page 15, applicants further disclose that a SiGe epi layer 40 is formed in the bipolar opening by the deposition of SiGe atop an exposed substrate surface 10, where oxide materials are not present. Applicant further disclose the deposition variables for forming the SiGe polysilicon layer 42:

> "SiGe layers and are formed in the present invention by utilizing a deposition process, wherein the deposition temperature is low, i.e., less than 900°C. More specifically, the deposition temperature used in this step of the present invention is from about 400° to about 500°C." *See* Page 15.

Applicants have disclosed that depositing SiGe over an oxide-containing region using the above process variables forms SiGe polysilicon. Therefore, applicants have disclosed to one of ordinary skill within the art how to make the SiGe polysilicon layers and respectfully request that the instant §112 rejection be withdrawn. Applicants note that the SiGe polysilicon layers may also be referred to as poly SiGe.

Claims 24-26 stand rejected under 35 U.S.C. §102(e) as allegedly anticipated by U.S. Patent No. 6,251,720 to Thakur, et al. ("Thakur, et al."). Claim 27 stands rejected under 35 U.S.C. §102(e) as allegedly anticipated or, in the alternative, under 35 U.S.C. §103 as allegedly unpatentable over Thakur, et al. Claim 28 stands rejected under 35 U.S.C. §103 as allegedly unpatentable over the combination of Thakur, et al. and U.S. Patent No. 6,150,701 to Lee ("Lee").

In regard to the anticipation rejections, it is axiomatic that anticipation under §102 requires that the prior art reference disclose every element of the claim to which it is applied. In re King, 801 F.2d 1324, 1326, 231 USPQ 36, 138 (Fed. Cir. 1986). Thus, there must be no differences between the subject matter of the claims and the disclosure of the applied prior art reference. Stated in another way, the reference must contain within its four corners adequate

direction to practice the invention as claimed. The corollary of this rule is equally applicable. The absence from the applied reference of any claimed element negates anticipation. Kolster Speedsteel AB v. Crucible Inc., 793, F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that Claims 24-27 are not anticipated by the disclosure of Thakur, et al. since the applied reference does not disclose applicants' claimed poly-poly capacitor which comprises *planar* upper and lower plate electrodes that are separated by an insulator structure, wherein at least the *planar* upper plate electrode is composed of SiGe polysilicon and said *planar* upper plate electrode is located directly above said insulator structure and said lower plate electrode is located directly below said insulator structure. In contrast, the capacitor structure disclosed in Thakur, et al., referring to FIG. 1F, comprises a non-planar lower electrode 104, non-planar upper electrode 106, and capacitor dielectric layer 102. Hence, the capacitor structure of the applied prior art fails to teach a poly-poly capacitor having a *planar* upper and lower electrode, as recited in amended Claim 1.

The foregoing remarks clearly establish that the disclosure of Thakur, et al. do not teach every aspect of the rejected claims, as required by King and Kolster Speedsteel; therefore the claims of the present application are not anticipated by the disclosure of Thakur, et al. Applicants thus submit that the since the instant §102(e) rejections have been obviated, the rejections to Claims 24-27 citing Thakur, et al. can and should be withdrawn.

In regard to the §103 rejections citing Thakur, et al. alone, or the combination of Thakur, et al. and Lee, applicants submit that the applied references do not render the claims obvious since Thakur, et al. alone, or Thakur, et al. in combination with Lee, do not teach or suggest applicants' claimed poly-poly capacitor structure. Specifically, the principal reference spurring each §103 rejections, i.e., Thakur, et al., is deficient for the same reasons as

mentioned hereinabove; therefore applicants incorporate those remarks herein by reference. To reiterate: Thakur, et al. do not teach or suggest a poly-poly capacitor structure which comprises *planar* upper and lower plate electrodes that are separated by an insulator structure, wherein at least the *planar* upper plate electrode is composed of SiGe polysilicon and said *planar* upper plate electrode is located directly above said insulator structure and said lower plate electrode is located directly below said insulator structure, as recited in amended Claim 24. In contrast, the capacitor structure disclosed in Thakur, et al. comprises a non-planar lower electrode 104, non-planar upper electrode 106, and capacitor dielectric layer 102. As stated above, the capacitor structure of the applied prior art applied prior art fails to teach a poly-poly capacitor having a *planar* upper and lower electrode, as recited in amended Claim 1.

The applied secondary reference, i.e., Lee, does not alleviate the above mentioned defects in Thakur, et al. since Lee also does not teach or suggest applicants' claimed poly-poly capacitor structure which comprises *planar* upper and lower plate electrodes that are separated by an insulator structure, wherein at least the upper plate electrode is composed of SiGe polysilicon.

Lee discloses a semiconductor device which includes a substrate having a plurality of device isolation regions, first and second n-wells horizontally spaced apart from either of the plurality of device isolation regions, a p-channel transistor formed in a second n-well, an input protection transistor horizontally spaced apart from the first n-well and the device isolation regions, on a symmetrical portion by the first n-well to the second n-well, and a guard ring formed between the first n-well and the input transistor. The disclosure of Lee does not, however, teach or suggest the presence of any capacitor structure, let alone the claimed poly-

poly capacitor structure wherein the upper plate electrode is *planar*, as recited in amended Claim 24.

The §103 rejections also fail because there is no motivation in the applied references which suggests modifying the structures described therein to include applicants' claimed poly-poly capacitor in which the *planar* upper plate electrode which is located atop an insulator structure is comprised of SiGe polysilicon. The rejections are thus improper since the prior art does not suggest this drastic modification. The law requires that a prior art reference provide some teaching, suggestion, or motivation to make the modification obvious. In re Fritch, 972 F.2d, 1260,1266, 23 USPQ 1780,1783-84 (Fed. Cir. 1992).

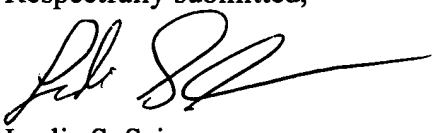
Here, there is no motivation provided in the disclosures of the applied prior art references, or otherwise of record, which would lead one skilled in the art to make the modification mentioned hereinabove. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d, 1260,1266, 23 USPQ 1780,1783-84 (Fed. Cir. 1992).

There is no suggestion in the prior art of applicants' claimed poly-poly capacitor structure therefore all the claims of the present application are not obvious from Thakur, et al., alone, as well as the combination of Thakur, et al. and Lee.

Based on the above amendments and remarks, the §103 rejections citing Thakur, et al., or Thakur, et al. and Lee have been obviated; therefore reconsideration and withdrawal of the instant §103 rejections are respectfully requested.

Wherefore reconsideration and allowance of the claims of the present application are respectfully requested.

Respectfully submitted,



Leslie S. Szivos
Registration No. 39,394

SCULLY, SCOTT, MURPHY & PRESSER
400 Garden City Plaza
Garden City, New York 11530
(516) 742-4343
LSS:HAH:jy